WHAT IS CLAIMED IS:

1. A method of pixel filtering for CMOS imagers, comprising:

scanning each of a plurality of pixels within a block;

designating a pixel as a process pixel, the process pixel having adjacent pixels, the process pixel having a process pixel value, each of the adjacent pixels having an adjacent pixel value; and

comparing the process pixel value to at least one adjacent pixel value.

2. The method of claim 1 further comprising detecting a lowest pixel value among the adjacent pixels.

3. The method of claim 2 wherein comparing compares the process pixel value to a lowest pixel value.

4. The method of claim 3 further comprising resetting the process pixel to a new pixel value.

5. The method of claim 4 wherein the new pixel value is the average pixel value of the adjacent pixel values.

6. The method of claim 1 further comprising detecting a highest pixel value among the adjacent pixels.

7. The method of claim 6 wherein comparing compares the process pixel value to a highest pixel value.

8. The method of claim 7 further comprising resetting the process pixel value when the process pixel value is a predetermined value lower than the lowest pixel value.

9. The method of claim 3 further comprising resetting the process pixel value when the process pixel value is a predetermined value greater than the highest pixel value.

10. The method of claim 1 further comprising exposing an array to a light source so as to cast an image on the array, the array having at least one block.

11. The method of claim 10 wherein the array is generally grid-shaped.

12. The method of claim 1 wherein the block is generally grid-shaped.

13. The method of claim 12 wherein the block has nine pixels.

14 A chip that automatically filters defective pixels in a CMOS imager, comprising:

a plurality of registers; and

filter logic coupled to the registers.

15. The chip of claim 14 wherein the filter logic is capable of:

designating a pixel as a process pixel, the process pixel having adjacent pixels, the process pixel having a process pixel value, each of the adjacent pixels having an adjacent pixel value; and

comparing the process pixel value to at least one adjacent pixel value.

16. The chip of claim 15 further comprising an array coupled to the registers.

17. A method of on-chip pixel filtering for CMOS imagers, comprising:

scanning each of a plurality of pixels within a block for a pixel value;

loading a pixel value into a register;

using filter logic to designate a pixel as a process pixel, the process pixel having adjacent pixels, the process pixel having a process pixel value, each of the adjacent pixels having an adjacent pixel value; and

using filter logic to compare the process pixel value to at least one adjacent pixel value.

18. The method of claim 17, wherein the filter logic compares the process pixel value to a highest pixel value, further comprising:

detecting the highest pixel value among the adjacent pixels; and

resetting the process pixel value to a new process pixel value when the process pixel value is a predetermined value higher than the highest pixel value.

19. The method of claim 1, wherein the filter logic compares the process pixel value to a lowest pixel value, further comprising:

detecting the lowest pixel value among the adjacent pixels; and

resetting the process pixel value to a new process pixel value when the process pixel value is a predetermined value lower than the lowest pixel value.

20. The method of claim 19 wherein the new process pixel value is the average pixel value of the adjacent pixel values.